Electronic Version
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Claims

[c1] 1. An electrostatic discharge (ESD) protection device for bypassing an ESD current between a first pad and a second pad, comprising:
a detection device, for detecting the ESD current, the detection device being connected between the first pad and the second pad, wherein the detection device comprises a diode and a variable resistor tuned by a diode, and an output terminal of the detection device is connected to the variable resistor; and
a clamp device, for bypassing the ESD current, the clamp device is connected between the first pad and the second pad and connected to the output terminal of the detection device;
wherein when the ESD current from the first pad or the second pad is detected by the detection device, a trigger voltage is generated to trigger the clamp device to bypass the ESD current due to a resistance of the variable resistor is changed by the diode.

[c2] 2. The ESD protection device of claim 1, wherein the first pad and the second pad comprise a VDD pad and a VSS pad, or the first pad and the second pad comprise a VSS

pad and a VDD pad.

[c3] 3. The ESD protection device of claim 1, wherein the detection device comprises a first N-type metal oxide semiconductor (NMOS) transistor comprising a drain connected to the first pad, a source connected to the output terminal of the detection device, a substrate connected to the second pad, and a gate connected to an output terminal of the diode, wherein an input terminal of the diode is connected to the second pad, and the variable resistor is connected between the output terminal of the detection device and the second pad.

[c4] 4. The ESD protection device of claim 3, wherein the detection device comprises a capacitor connected between the first pad and the gate of the first NMOS transistor, and a resistor connected between the second pad and the gate of the first NMOS transistor.

[c5] 5. The ESD protection device of claim 3, wherein the clamp device comprises a second NMOS transistor comprising a drain connected to the first pad, a source connected to the second pad, a substrate connected to the output terminal of the detection device, and a gate connected to the substrate of the second NMOS transistor or the second pad.

[c6] 6. The ESD protection device of claim 3, wherein the detection device comprises a bipolar PNP transistor comprising an emitter connected to source of the first NMOS transistor, a base connected to the second pad, and a collector connected to the output terminal of the detection device.

[c7] 7. The ESD protection device of claim 6, wherein the clamp device comprises a second NMOS transistor comprising a drain connected to the first pad, a source connected to the base of the bipolar PNP transistor, a substrate connected to the output terminal of the detection device and a gate connected to the second pad.

[c8] 8. The ESD protection device of claim 6, wherein the detection device comprises a capacitor connected between the first pad and the gate of the first NMOS transistor, and a resistor connected between the second pad and the gate of the first NMOS transistor.

[c9] 9. The ESD protection device of claim 1, wherein the clamp device comprises a second NMOS transistor comprising a drain connected to the first pad, a source connected to the second pad, a substrate connected to the output terminal of the detection device, and a gate connected to the substrate of the second NMOS transistor or the second pad.

[c10] 10. An electrostatic discharge (ESD) protection circuit for bypassing an ESD current between a first pad and a second pad, comprising:

a P-type substrate;

a diode, comprising a N-well region in the substrate and a N+ region in the N-well region;

a N-type metal oxide semiconductor (NMOS) transistor, comprising a drain region in the substrate and connected to the first pad, a source region in the substrate and connected to the second pad, and a gate formed over a portion of the drain region, a portion of the source region and the substrate there-between; and

a first P+ region, formed in the substrate between the N-well region and the source region of the NMOS transistor, and a second P+ region formed in the substrate at the other side of the N-well region, wherein the gate region of the NMOS transistor is connected to the first P+ region or the second P+ region and the second P+ region is connected to the second pad;

wherein when the ESD current from the first pad or the second pad is detected, a trigger voltage is generated to trigger the NMOS transistor to bypass the ESD current due to a resistance of substrate around the N-well is changed by the diode.

[c11] 11. The ESD protection circuit of claim 10, wherein the first pad and the second pad comprise a VDD pad and a VSS pad, or the first pad and the second pad comprise a VSS pad and a VDD pad.

[c12] 12. The ESD protection circuit of claim 10, further comprising:
another NMOS transistor comprising a drain region connected to the first pad, a source region connected to the first P+ region, a substrate region connected to the second pad and a gate region connected to the N+ region of the N-well.

[c13] 13. The ESD protection circuit of claim 12, further comprising:
a capacitor, connected between the first pad and the gate region of the another NMOS transistor, and a resistor connected between the second pad and the gate region of the another NMOS transistor.

[c14] 14. The ESD protection circuit of claim 12, wherein when the gate region of the NMOS transistor is connected to the second P+ region, further comprising:
a bipolar PNP transistor, comprising an emitter connected to the first P+ region, a base connected to the source region of the NMOS transistor, and a collector connected to a portion of the substrate under the first

P+ region and the source region of the NMOS transistor.

[c15] 15. The ESD protection circuit of claim 14, further comprising:

a capacitor, connected between the first pad and the gate region of the another NMOS transistor, and a resistor connected between the second pad and the gate region of the another NMOS transistor.